

# A FPGA-based design methodology for digital predistortion of power amplifiers

Metodología de diseño basada en FPGA  
para la predistorsión digital de amplificadores de potencia

José Alejandro Galaviz-Aguilar,<sup>1\*</sup> José Ricardo Cárdenas-Valdez,<sup>1</sup>  
J. Apolinar Reynoso-Hernández,<sup>2</sup> Christian Gontrand,<sup>3</sup> José Cruz Núñez-Pérez<sup>1</sup>

<sup>1</sup> Centro de Investigación y Desarrollo de Tecnología Digital, Instituto Politécnico Nacional.  
Av. Instituto Politécnico Nacional 1310, Mesa de Otay, CP 22150, Tijuana, BC, México.

<sup>2</sup> Centro de Investigación Científica y de Educación Superior de Ensenada. Carretera Ensenada-Tijuana 3918,  
Zona Playitas, CP 22860, Ensenada, BC, México.

<sup>3</sup> Université de Lyon. INSA-Lyon, INL, CNRS UMR5270, Villeurbanne, F-69621, France.

\* E-mail: jgalaviz@citedi.mx

## KEYWORDS:

power amplifier, FPGA, digital predistortion, linearization, lookup table.

## ABSTRACT

This paper describes the design and implementation of a memoryless digital predistortion (DPD) system for the linearization of power amplifiers. The system prototype predistorter requirements and architecture are implemented over a DSP-FPGA development kit. The design methodology is described in practical blocks and analyzed in detail with special emphasis in the digital domain, where the algorithms proposed are implemented. The approach of the predistorter system is based in a complex lookup table to program the inverse AM-AM and AM-PM conversion curves of the power amplifier.

## PALABRAS CLAVE:

amplificador de potencia, FPGA, predistorsión digital, sistema lineal, tabla de búsqueda.

## RESUMEN

Este artículo describe el diseño e implementación de un sistema de predistorsión digital (DPD) sin memoria para la linealización de amplificadores de potencia. El prototipo del sistema y la arquitectura se implementaron usando un kit de desarrollo DSP-FPGA. La metodología de diseño es descrita en bloques prácticos y analizada en detalle con énfasis especial en el dominio digital, donde se ejecutaron los algoritmos propuestos. La estrategia del sistema predistorsionador está basada en una tabla de búsqueda compleja que permite programar las curvas de conversión inversas de AM-AM y AM-PM de un amplificador de potencia.

## 1 INTRODUCTION

The distortion of signals in communication systems is attributed to the nonlinear characteristics of components such as the radio frequency (RF) power amplifier (PA). To minimize this nonlinearity effect in the signal the predistortion technique requires a nonlinear module. In this technique, the signal provided to the amplifier is altered by generating a compensation characteristic that is the opposite to the transfer characteristic of the amplifier, in both amplitude and phase, and this altered signal is provided to the amplifier. As a consequence, the linear operation is preferably extended into higher levels and the intermodulation products are removed or at least reduced. The election of the digital predistortion approach is possible due to its linearity growth, obtaining a marked improvement in the efficiency and reducing the size and cost of the transmitter system. The digital approach of the implemented predistorter in the Field-Programmable Gate Array (FPGA) combines hardware and software co-design techniques in order to optimize the design blocks of the predistorter system [1].

## 2 DESIGN AND IMPLEMENTATION OF DIGITAL PREDISTORTION

The basic concept of a digital predistortion (DPD) system is to distort the baseband signal previous to the modulation and the PA stage, so that the total result system performance is linear [2]. The system is illustrated in Figure 1.

The signal to be transmitted is represented by its complex envelope  $x = I + jQ$ , where  $x$  is

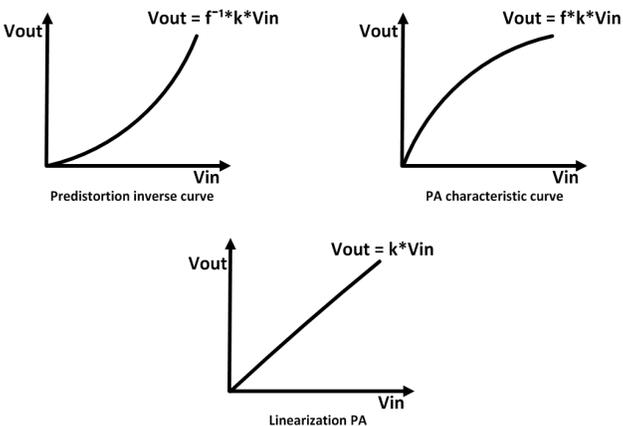


Figure 1. Digital predistortion concept in amplitude

the complex signal with  $I$  “In-phase” and  $Q$  “Quadrature” components, respectively. It is suitably modified by a predistortion function in order to produce a predistorted signal [3]. The design implementation of a digital predistorter is integrated into the architecture of a digital signal processor (DSP) development kit, Altera Cyclone III. Figure 2 shows the block diagram of the overall system.

An analog test bed covers a necessary stage for the characterization of the complete system. The digital design approach is based on the resources of the FPGA and the data conversion High Speed Mezzanine Card (HSMC). The FPGA-based predistorter in the FPGA represents a nonlinear module located previous to the RFA stage. The design considers several design blocks, as shown in Figure 3.

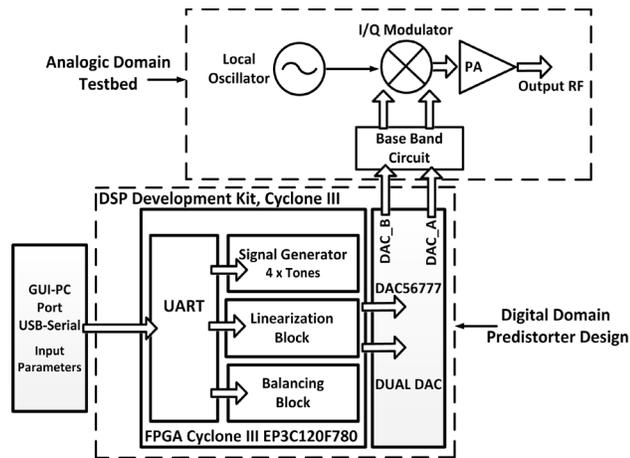


Figure 2. Overall system

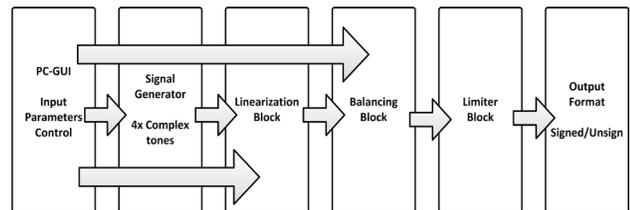


Figure 3. Digital predistorter design blocks

### 2.1 Signal generator block

The signal generator block is based on a direct digital synthesis technique, which consists in generating a periodic and discrete-time waveform of known frequency  $F_o$ . [4]. The project implements the signal generator block in the FPGA, it is a top-level design developed with the Quartus II FPGA design software tool. The synthesis tool generates the primitive logic,

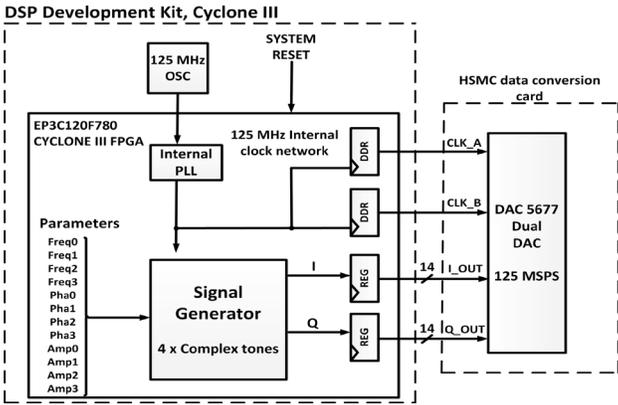


Figure 4. Signal generator schematic

connections, and components from the generic file of synthesizable source-code in very-high-speed integrated circuits hardware description language (VHDL), which is based in structural modeling.

The phase-locked loop (PLL) component generates the internal 125 MHz clock signal, obtained from the oscillator input on the FPGA board and is the reference clock into the FPGA. This clock internally generated by the PLL also acts as the internal clock network that feeds the FPGA logic circuitry. The differential clock signals driven to the outputs of the Digital to Analog Converter (DAC) are used as sampling clock of DAC\_A and DAC\_B channels on the HSMC card [5]. The custom design is illustrated in Figure 5; it consists of a complex sinusoidal function generator able to create a signal which could reach until four tones with programmable values of output frequencies (phase\_inc0, phase\_inc1, phase\_inc2, phase\_inc3) and phase corrections (phase\_shift0, phase\_shift1, phase\_shift2, phase\_shift3), implemented in a design with four programmable components, which are 12-bits resolution numerically controlled oscillators (NCO). This block allows the system to obtain a complex signal in the output, expressed by the following equation:

$$x = A \sin(\omega t + \varphi) = I \cos(\varphi) + Q \sin(\varphi) \quad (1)$$

The sine and cosine output waveforms in the NCO component are multiplied by an amplitude value with length 8-bit signed. This value is in the format "s3.4": 1 sign bit, 3 bits for the integer part and 4 bits to represent the fractional part (see Table 1).

A modified universal asynchronous receiver/transmitter (UART) module is configured to allow the sending of 8-byte format packets to transmit a serial

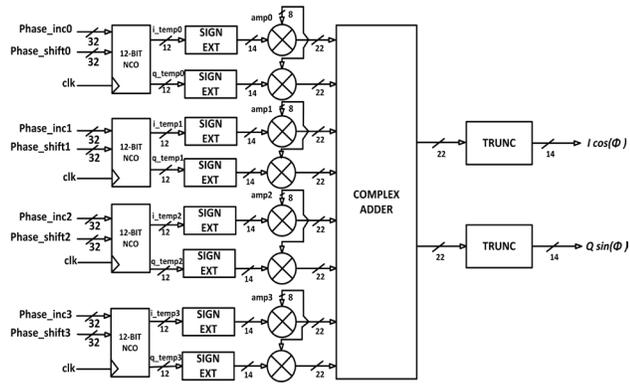


Figure 5. Complex signal generator design

Table 1. Scale factor amplitude

(REAL) SCALE FACTOR	(BINARY) SCALE FACTOR	(HEX) SCALE FACTOR	NOTE
7.9375	0111.1111	0x7F	Max +
0.0625	0000.0001	0x01	Min -
0.0	0000.0000	0x00	Amp 0
-8.0	1000.0000	0x80	Max -

data stream that is used to control and reprogram all the register values. The header byte is composed of 3 unique bytes; the register map control stores all the register values of frequency, phase shifts, amplitudes, linearization parameters, and balancing parameters, which are conducted directly to the FPGA design. Figure 6 shows the packet format structure.

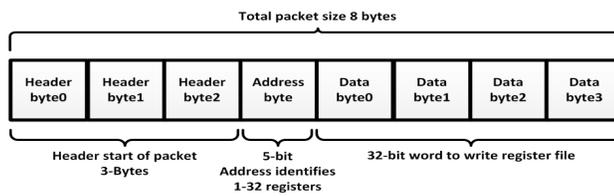


Figure 6. 8-bytes packet format

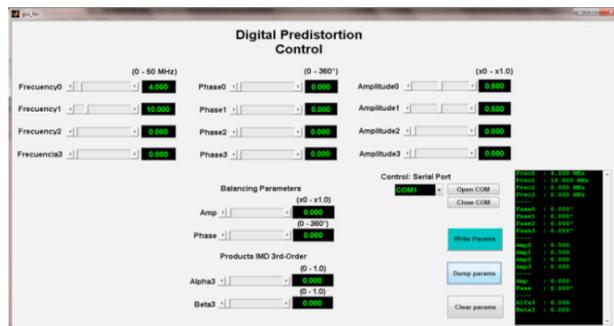


Figure 7. Matlab GUI to control input parameters

The register file in the FPGA is programmed via the USB-to-serial converter device, connected to the PC. The USB-to-serial module is configured as a simple COMX serial port. To write the bytes into the register file in the project a graphical user interface (GUI) was developed in Matlab software, to control the input parameters in a simple form through the FPGA design; Figure 7 illustrates the developed Matlab GUI.

## 2.2 Linearization block

This block produces a signal to compensate the nonlinear intermodulation distortion (IMD) caused in the PA stage as a result of two or more signals interacting in a nonlinear device. The quasi-memoryless distorted function modifies the phase and amplitude of the input signal to compensate the AM-AM and AM-PM distortions introduced by the PA, where the output of the linearizer block should be the following expression [6]:

$$y = AB \sin(\omega t + \varphi + \psi) = I_{pd} \cos(\varphi) + Q_{pd} \sin(\varphi) \quad (2)$$

The parameters  $I_{pd}$  and  $Q_{pd}$  are given by the following matrix:

$$\begin{bmatrix} I_{pd} \\ Q_{pd} \end{bmatrix} = \begin{bmatrix} \beta \cos(\psi) & -\beta \sin(\psi) \\ \beta \sin(\psi) & \beta \cos(\psi) \end{bmatrix} = \begin{bmatrix} \alpha(t) & -\beta(t) \\ \beta(t) & \alpha(t) \end{bmatrix} * \begin{bmatrix} I \\ Q \end{bmatrix} \quad (3)$$

The linearization block is based on the algorithm exhibited in Figure 8.

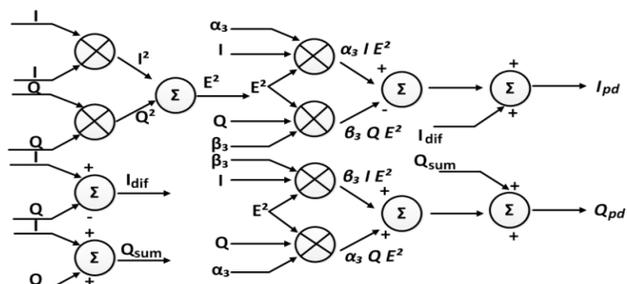


Figure 8. Linearization algorithm

The 3rd order memoryless algorithm uses the envelope  $E^2$  to evaluate the predistortion coefficients, for  $\alpha_3$  and  $\beta_3$ . The values of the vector  $I$  and  $Q$  vary in magnitude (modulus) with regard to the amplitude modulation of the input signal, expressed as follows:

$$E^2 = \sqrt{I^2 + Q^2} \quad (4)$$

The coefficients  $\alpha$  and  $\beta$  are real input values used to cancel the 3rd order intermodulation that is generated for nonlinearities, which are expressed by the following equations:

$$\alpha(t) = 1 + \alpha_2 E + \alpha_3 E^2 \quad (5)$$

$$\beta(t) = 1 + \beta_2 E + \beta_3 E^2 \quad (6)$$

These coefficients are used to minimize the adjacent channel power ratio (ACPR) and to obtain multiple sinusoidal excitations.

$$I_{pd} = I + \alpha_3 I E^2 - Q - \beta_3 Q E^2 \quad (7)$$

$$Q_{pd} = I + \beta_3 I E^2 + Q + \alpha_3 Q E^2 \quad (8)$$

## 2.3 Balancing block

This block allows correcting the distortions of the modulator imbalance in vectors  $I/Q$ . The  $I/Q$  modulator is a crucial component that is placed before the RF power amplifier and performs the mixture of  $I$  and  $Q$  signals for an RF input to be amplified by the PA. The degradation in accuracy of the  $I$  and  $Q$  vectors is due to noise, and offset in the amplitude (AM) and phase modulation (PM) [7]. Therefore, this block is considered in the configuration of two parameters, amplitude ( $\Delta A$ ) and phase ( $\Delta \varphi$ ). The method for balancing the amplitude and phase is based on the algorithm expressed in Figure 9 [8-10].

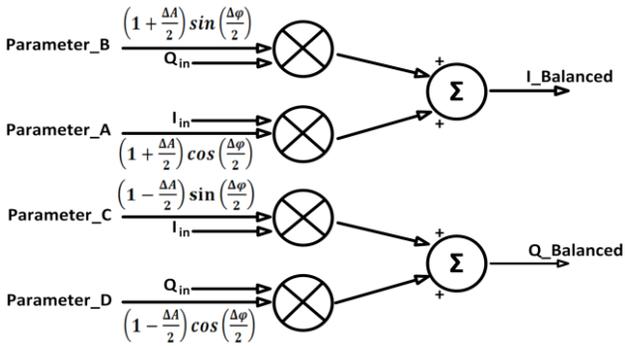


Figure 9. Balancing algorithm

Where we can define with the following expressions:

$$I_{ba} = Param_A * I_{en} + Param_B * Q_{en} \quad (9)$$

$$Q_{ba} = Param_C * I_{en} + Param_D * Q_{en} \quad (10)$$

$$Param_A = \left(1 + \frac{\Delta A}{2}\right) \cos\left(\frac{\Delta \varphi}{2}\right) \quad (11)$$

$$Param_B = \left(1 + \frac{\Delta A}{2}\right) \sin\left(\frac{\Delta \varphi}{2}\right) \quad (12)$$

$$Param_C = \left(1 - \frac{\Delta A}{2}\right) \cos\left(\frac{\Delta \varphi}{2}\right) \quad (13)$$

$$Param_D = \left(1 - \frac{\Delta A}{2}\right) \sin\left(\frac{\Delta \varphi}{2}\right) \quad (14)$$

The parameters (Param\_A, Param\_B, Param\_C and Param\_D) are mathematical expressions with coefficients  $\Delta A$  and  $\Delta \varphi$ . In the project design they are assigned as four input values 14-bit signed, with an assumed "s13" format, with 1 sign bit and 13 fraction bits, where  $\Delta A$  is the adjustment in amplitude of the  $I/Q$  vectors, and  $\Delta \varphi$  is the phase difference between the  $I/Q$  vectors.

## 2.4 Limiter block

This block is designed to limit the dynamic range of the transmitted signal to avoid saturation. Basically the limiter sets an active range of voltage in the output signals to be transmitted, the signal is restricted within a certain voltage value peak to peak, and it can neither exceed the maximum condition nor go below the minimum voltage. The limiter involves two 14-bit inputs,  $I_{in}$  [13..0],  $Q_{in}$  [13..0] and two 14-bit outputs  $I_{out}$  [13..0] and  $Q_{out}$  [13..0]. The algorithm applied to  $I$  and  $Q$  signals is identical and verifies the insertion of the two comparator signal functions  $I$  (*cosine*) and  $Q$  (*sine*) where it makes a comparison of the maximum and the minimum value. If the signed comparator output is true, the result is assigned to a multiplexer to determine the output of the limiter block (see Figure 10). The limiter block design considers that Quartus II software tool is based on bits. This leads to make changes in the input parameters representation, because the database should be converted to binary "bits" instead of decimal numbers, since the output should be limited with a length of 14 bits, which makes it necessary to limit the signal range  $\pm 8191 \cdot 2^{14} - 1 = 16384/2 - 1 = 8191$ . For comparison, the maximum value is set at 8191, and the minimum value is set to 253,953, which is -8191 represented in an 18 based number system. For the multiplexer, the maximum value is set at 8191, and the minimum value is set at 8193, which is -8191 in a 14 based number system.

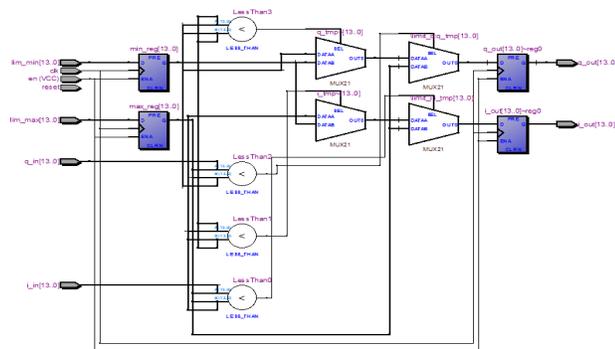


Figure 10. Limiter register transfer level

## 2.5 Output format

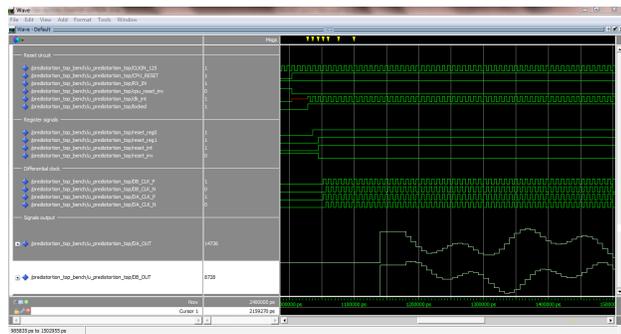
The sign-unsigned block outputs are sent directly to the analog test bed system. Due to the design of DPD in previous blocks, where sign signals are required to perform various arithmetic operations, a VHDL file is needed to change the output format of the data to the DAC channels A and B; this is achieved inverting the sign bit from '1' and allows performing an offset binary (unsigned), as shown in Table 2. "Offset binary" representation provides an unsigned format to assign the data to the inputs DAC 14-bit. The block format is described by a source code file written in VHDL.

**Table 2.** FPGA pin assignments

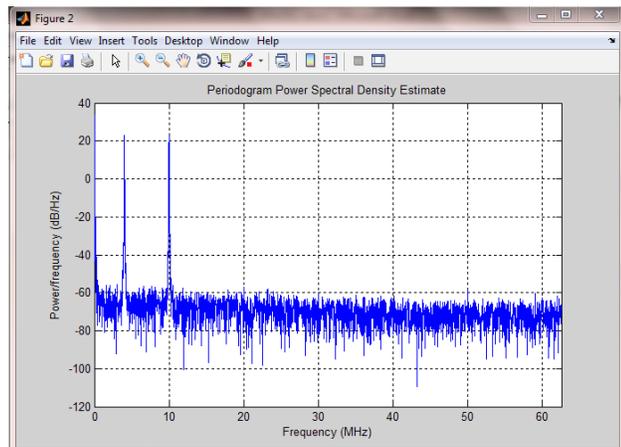
Pin name	I/O	Description	Active state
clk	in	sample clock	rising edge
reset	in	asynchronous reset signal	active-low
en	in	active state clock	active-high
phase_inc0-3 [31:0]	in	phase increment un-signed 32-bit	data
phase_shift0-3 [31:0]	in	phase shift unsigne 32-bit	data
amp0-3 [7:0]	in	waveform amplitude	data
i_out	out	14-bit output (Chanel I)	data
q_out	out	14-bit output (Chanel Q)	data
output format	in	control params outputs I/Q	0 comp2 1 binary offset

## 3 RESULTS

A simulation register-transfer level (RTL) of the signal generator hardware was described in a VHDL testbench and run in Modelsim software, the hardware test shows a signals part of the internal design and a verification of output waveforms of two programmable tones at 4 MHz and 10 MHz from the signal generator block. The simulation test is illustrated in Figure 11.



**Figure 11.** VHDL hardware simulation of two tones at 4 and 10 MHz



**Figure 12.** FFT plot of two output tones at 4 and 10 MHz

**Table 3.** FPGA utilization

Block	DSP Elements (Embedded Multipliers)	Dedicated Logic Registers	Memory bits	Logic Elements
Signal generator	16	312	393216	364
Linearization	16	84	56	163
Balancing	8	28	0	54
Limiter	0	56	0	101
Output format	0	28	0	29
Register	0	438	0	459
UART	0	112	0	150
Total used	40	1366	393272	1790
Available in FPGA	576		3981312	119088
Percent used	7%		10%	2%

The Matlab results are shown in Figure 12. Two complex tones improve the spectral purity and spurious free dynamic range (SFDR) from 80 dB in reference with the output tones and a spectral power of 20 dBm.

The overall resources used in the FPGA for the digital predistorter design are summarized in Table 3, where the resources necessary for each module of the implemented design are noted in detail.

#### 4 CONCLUSION

This paper described a comprehensive methodology for the design of an implemented DPD architecture based on a DSP development kit of Altera. This enables DPD characterization of a testbed to achieve RFA linearization considering nonlinear defects present in the PA. This is achieved by integrating and balancing linearization algorithms in a digital design with a feedback prototype in order to correct the system output. The contribution of this prototype resides in the theoretical integration of digital predistortion algorithms considering physical and mathematical models present in the PA, representing their actual behavior.

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*About the authors*



José Alejandro Galaviz Aguilar was born in Delicias Chihuahua, Mexico, in March 27, 1985. He received his Engineering degree from the Northern University Studies Center in Delicias, Chihuahua, Mexico, in 2010, and the MSc degree in Digital Systems from the Digital Technology Research and Development Center of National Polytechnic Institute (CITEDI-IPN) in Tijuana, Mexico, in 2013. He is currently working to reach his Ph.D. degree in CITEDI-IPN. His research interests include design and modeling of digital algorithms for the linearization of devices, mainly power amplifiers, and the design of components for digital communications systems and system-level design using FPGA devices.



José Ricardo Cárdenas-Valdez was born in Tijuana, Baja California, Mexico, in October 1, 1982. He received his Engineering degree from the Tijuana Technological Institute (ITT) in Baja California, Mexico, in 2006, and his MSc degree in Digital Systems from the Digital Technology Research and Development Center of National Polytechnic Institute (CITEDI-IPN), in Tijuana, Mexico, in 2008. He is currently working to reach his Ph.D. degree in CITEDI-IPN. His research interests include design and modeling of digital and analog devices, mainly power amplifiers, high frequency devices and FPGA design.



J. Apolinar Reynoso-Hernández received the Electron. Telecommun. Eng. degree from ESIME-IPN, Mexico, the M.Sc. degree in solid state physics from CINVESTAV-IPN, Mexico and the Ph.D. degree in electronics from the Université Paul Sabatier-LAAS du CNRS, Toulouse, France, in 1980, 1985, and 1989, respectively. His doctoral thesis was on low-frequency noise in MESFET and HEMTs. Since 1990, he has been a researcher with the Electronics and Telecommunications Department of CICESE, Ensenada, Baja California, Mexico. His areas of specialized research interest include high-frequency on-wafer measurements, high-frequency device modeling, linear, nonlinear and noise device modeling, and switched power amplifiers. He was the recipient of ARFTG's best paper poster award in 2001 and 2012.



Christian Gontrand has MS, PhD and State Doctorat degrees. From 1982 to 1984, he was part of Thomson's Laboratoire Central de Recherche. From 1988 on, he joined the Laboratoire de Physique de la Matière. From 1988 to 1996, he was in charge of the technical area of the new Centre de Microélectronique de la Région Lyonnaise and worked on new RF devices, with CNET. From 1997 to 2001, as a professor, he was the head of the team Smart System Integration, at the Centre de Génie Electrique. From 2002 on, he has lead the team RF Systems of the Lyon Institute of Nanotechnology, 3D circuits.



José Cruz Núñez Pérez received his MSc degree in electronics engineering from the National Center of Research and Technological Development (CENIDET), in Cuernavaca, Mexico, in 2003, and his PhD degree from the Institut National des Sciences Appliquées de Lyon (INSA-Lyon), Villeurbanne France, in 2007. In first semester 2008, he was a Research Director at Advanced Technology Research SA de CV (ATR) in Guadalajara, Mexico, where he led a team of researchers working on networking and telecommunication architectures. Since August 2008, he has been a professor at the Digital Technology Research and Development Center of National Polytechnic Institute (CITEDI-IPN), in Tijuana, Mexico. He is the Research Coordinator in the Telecommunications Department at CITEDI. His research interests include digital and analog circuits design, device physic modeling, DSP and FPGA design.